UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, vs. SAMSUNG ELECTRONICS CO, LTD; SAMSUNG ELECTRONICS AMERICA, INC.; SAMSUNG SEMICONDUCTOR INC., Defendants.	Case No. 2:22-cv-293-JRG JURY TRIAL DEMANDED (Lead Case) [redacted]
NETLIST, INC., Plaintiff, vs. MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC. Defendants.	Case No. 2:22-cv-294-JRG JURY TRIAL DEMANDED

PLAINTIFF NETLIST INC.'S OPPOSITION TO SAMSUNG'S MOTION FOR PARTIAL SUMMARY JUDGMENT REGARDING ITS ABSOLUTE INTERVENING RIGHTS DEFENSE

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I. INTRODUCTION

Samsung seeks summary judgment that all asserted claims of the '912 patent except for claim 16 are subject to absolute intervening rights based on amendments to the claims during the reexamination of the '912 patent. Dkt. 81 at 1. Samsung is not entitled to summary judgment of intervening rights for the original claims of the '912 patent amended during reexamination: 1, 3, 4, 6, 8, 10, 11, 15, 18, 19, 20, 22, 24, 27-29, 31, 32, 34, 36-39, 40, 41, 43, 45-47 and 50 (the "Amended Claims"). These claims were also at issue in *Netlist Inc. v. Google LLC*, Case No. 4:09-cv-5718 (N.D. Cal.). The N.D. Cal. Court held that the Amended Claims are subject to intervening rights. Dkt. 81-08 at 44. However, the N.D. Cal. Court gave undue weight to the fact that the claims were amended to overcome the prior art, and did not consider Samsung's IPR arguments in a co-pending IPR involving the '912 patent, which shed light on the interpretation of terms in the original claims.[1] Under a proper interpretation of the original claims, Samsung is not entitled to intervening rights with respect to these claims because the Amended Claims are "substantially identical" in scope to the original claims.

II. RESPONSE TO STATEMENT OF THE ISSUE

Whether Samsung's intervening rights defense fails as a matter of law because it has failed to demonstrate that the claims have substantively changed in scope under the *Phillips* standard.

III. RESPONSE TO STATEMENT OF UNDISPUTED MATERIAL FACTS

1, 11, 13-15. **Undisputed**.

2-10, 12. **Disputed**. Netlist disputes Samsung's characterization of Netlist's statements and amendments during reexamination. Netlist amended the original claims to clarify the meaning of claim limitations related to three components of the claimed memory module: the phase-lock loop ("PLL")

[1] IPR2022-00615 involves claim 16 of the '912 patent, which the N.D. Cal. Court held was not subject to intervening rights. Dkt. 81-08 at 44.

device, the register, and the logic element. Dkt. 81-01, at 48-49. These amendments were made to better define the claims and avoid what Netlist believed were overly broad constructions of the claims by the USPTO, which employed the expansive BRI standard throughout the reexamination. *See* Ex. 5 at 14-16. The amendments did not affect a substantive change. *See* Section IV.B.

16-17. **Disputed**. Netlist's November 17, 2022 preliminary infringement contentions ("PICs") asserted the Amended Claims against DDR2 FBDIMMs, DDR3 LRDIMMs and other DDR2/DDR3 products that "utilize on-module logic to perform rank multiplication." Dkt. 81-06 at 5. Netlist accused DDR3 RDIMMs in this latter category of products. *Id.* Yet, [redacted] Samsung's identification of products it contends are subject to intervening rights is deficient. *See* Section V.C.

IV. LEGAL STANDARD

Absolute intervening rights preclude liability for products that were purchased or used prior to the conclusion of reexamination. 35 U.S.C. § 252; pre-AIA § 316(b). The accused infringer must show that the amended claims are not "substantially identical" to the original claims for intervening rights to apply. 35 U.S.C. § 252.[2] "Identical" means "at most without substantive change." *Bloom Eng'g Co. v. N. Am. Mfg. Co.*, 129 F.3d 1247, 1250 (Fed. Cir. 1997). In determining whether an amendment is a substantive change, "[i]t is the scope of the claim that must be identical, not that identical words must be used." *Convolve, Inc. v. Compaq Comput. Corp.*, 812 F.3d 1313, 1322 (Fed. Cir. 2016).

[2] The Federal Circuit holds that intervening rights apply to amendments during reexamination even if the scope of the claims are narrowed. *Laitram Corp. v. NEC Corp.*, 163 F.3d 1342, 1349 (Fed. Cir. 1998). Netlist believes that this decision is inconsistent with the statutory language, but recognizes that this is an issue for the Federal Circuit. For the purposes of this motion, Netlist will apply *Laitram*.

V. ARGUMENT

A. Netlist is Not Judicially Estopped from Contesting Intervening Rights

Samsung contends that Netlist is estopped from contesting intervening rights based on the USPTO's determination during the reexamination of the '912 patent that the Amended Claims were patentable. Dkt. 81 at 6-8. At least "[t]wo elements are necessary for judicial estoppel: (1) the estopped party's position must be 'clearly inconsistent with its previous one,' and (2) 'that party must have convinced the court to accept that previous position.'" *Owens v. W. & S. Life Ins. Co., 717 F. App'x* 412, 417 (5th Cir. 2018) (citation omitted). Neither element is met here.

During reexamination, Netlist amended original independent claims 1, 15, 28, and 39 of the '912 patent. Dkt. 81-02 at 1:25-3:8, 3:44-5:25. Each of the independent claims originally recited a memory module comprising a "phase-lock loop device," ("PLL") a "register" and a "logic element" with certain specific operations. *Id.* The Examiner and Board applied the BRI standard throughout the reexamination. *See, e.g.*, Ex. 5 at 14-16 (Board affirming Examiner's broad construction of "logic element" under the BRI standard). Netlist amended these claims to add limitations clarifying the operation of the PLL, register, and logic element. *See* Dkt. 81-01 at 47-49.

Samsung argues that judicial estoppel should apply because it would be inconsistent for Netlist to argue that there have been no substantive changes to the original claims based on Netlist's statements to the USPTO and Federal Circuit that it "narrowed" its claims. Dkt. 81 at 6-8. Samsung ignores that these statements were made in reexamination, where the BRI standard applies. The BRI standard requires the USPTO to select the broadest of multiple reasonable interpretations in light of the specification. *Google LLC v. Network-1 Techs., Inc.*, 726 F. App'x 779, 785 (Fed. Cir. 2018) ("[U]nder the broadest reasonable construction standard, where two claim constructions are reasonable, the broader construction governs."). By contrast, the Federal Circuit has made clear that "[i]n the intervening rights analysis, [a court's] task is to interpret the scope of the claims per the *Phillips*

standard." *Convolve,* 812 F.3d at 1325 (reversing district court's intervening rights finding, noting "[t]o the extent that the district court adopted [the Examiner's] reasoning wholesale without accounting for the differences between the broadest reasonable interpretation standard and *Phillips*, the court erred").

Courts have declined to find positions inconsistent for purposes of judicial estoppel where those positions implicate different claim construction standards. For example, in *Research Frontiers*, the court declined to estop E Ink from advancing constructions that were different from those it had previously advanced during IPR, finding it was not inconsistent to advocate for one construction under the BRI standard and another under *Phillips*. *Rsch. Frontiers, Inc. v. E Ink Corp.*, 2016 WL 1169580, at *3, n.4 (D. Del. Mar. 24, 2016), *report and recommendation adopted*, 2016 WL 7217217 (D. Del. Dec. 13, 2016), *aff'd*, 706 F. App'x 685 (Fed. Cir. 2017). The court reasoned that "E Ink could reasonably—and not inconsistently—have argued that the constructions it proposed during the IPR proceeding amounted to the 'broadest reasonable interpretation' that the terms could support, and nevertheless now argue that, when taking into account guidance from cases like *Phillips*, the Court should adopt a different, narrower construction for the same terms." *Id.*; *see also Mike's Train House, Inc. v. Broadway Ltd. Imports, LLC*, 2012 WL 664498, at *22 (D. Md. Feb. 27, 2012) (inconsistency prong of judicial estoppel was not met where "Defendants' argument to the PTO … that the broadest reasonable interpretation of speed command covered functions disclosed in the prior art" was not "inconsistent with Defendants' argument at summary judgment that the accused trains do not accept speed commands under the more narrow construction that the parties have applied in this case."), *aff'd,* 500 F. App'x 958 (Fed. Cir. 2013). In the analogous context of collateral estoppel, the Federal Circuit has also relied on the difference between the BRI and *Phillips* standards to find that the issue of claim construction had not actually been litigated. *SkyHawke Techs., LLC v. Deca Int'l Corp.*, 828 F.3d 1373, 1376 (Fed. Cir. 2016) ("Because the Board applies the broadest reasonable construction of the claims while the district courts apply a different standard of claim construction as explored in [*Phillips*], the

issue of claim construction under *Phillips* to be determined by the district court has not been actually litigated.").

To be sure, Netlist stated in remarks accompanying the amendments and in its Federal Circuit brief that Netlist had "narrowed" the claims to include the PLL, register, and logic element amendments. Dkt. 81-01 at 51; Dkt. 81-05. This narrowing was from the BRI interpretation of the claim, whereas intervening rights requires an analysis of the scope of the amended claims vis-à-vis the original claims under the *Phillips* standard. *Convolve,* 812 F.3d at 1325. As the Federal Circuit instructed in *Convolve*, the absolute intervening rights inquiry "must focus on a case-by-case analysis of the scope of the claims before and after claim amendment." *Id.* at 1325. Indeed, the Federal Circuit declined to give significant weight to the patentee's and examiner's use of the term "clarify" or "clarifying," focusing instead on construing the original claims in light of the *Phillips* standard. *Id.* Given the fact-specific nature of this inquiry and the different claim construction standard it requires, Samsung's bid to short-circuit the analysis through judicial estoppel should be rejected.

As another independent reason for rejecting Samsung's judicial estoppel argument, there is no evidence that the Federal Circuit or PTAB relied on Netlist's statements to affirm the validity of the Amended Claims. The Federal Circuit issued a one-line order summarily affirming the PTAB. *See Google LLC v. Netlist, Inc.*, 810 F. App'x 902 (Fed. Cir. 2020). Similarly, the PTAB's decision affirming the validity of the Amended Claims makes no mention of Netlist's "narrowing" remarks. *See* Dkt. 81-04. And where the PTAB cited to Dr. Sechen's statements regarding the "narrower claim[s]," it noted that Dr. Sechen's comments were "confusing." *Id.* at 19.

B. The Amended Claims are "Substantially Identical" to the Original Claims under the *Phillips* Standard

Original independent claim 1 is representative of the original independent claims, which recited a "PLL," "register," and "logic element" as emphasized below.

> 1. A memory module connectable to a computer system, the memory module comprising:
>
> a printed circuit board;
>
> a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;
>
> a circuit mounted to the printed circuit board, the circuit comprising a **logic element and a register**, the **logic element** receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and
>
> a **phase-lock loop device** mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the **logic element**, and the **register**.

Ex. 1 ('912 patent), 32:59-33:27. In its July 31, 2016 amendment, Netlist amended the claims to include additional language regarding the "PLL," "register," and "logic element." Dkt. 81-01 at 48-49. These amendments did not substantively change the scope of the claims:

1. The "PLL" Amendment

Netlist added the following language regarding the operation of the PLL device: "wherein, in response to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register." Dkt. 81-01 at 48. The original claims required the PLL device be "operatively coupled to the plurality of DDR memory devices, the logic element, and the register." *See, e.g.*, Ex. 1 ('912 patent), 33:24-27 (claim

1), 34:53-57 (claim 15); *see also* 36:2-4 (claim 28); 36:49-53 (claim 39: "operationally coupled"). The specification teaches that the PLL is the source of clock signals for each of these components. *Id.*, 5:28-31 ("In response to signals received from the computer system, the phase-lock loop device 50 ***transmits clock signals to the plurality of memory devices 30, the logic element 40, and the register 60***.") (emphasis added); *see also* Figs. 1A-1B (output of PLL (50) is directly coupled to logic element (40), register (60), and plurality of DDR memory devices (30)).

Samsung argues that the PLL amendment affected a substantive change because "[t]he original claims did not require the PLL transmit any specific signal to the logic element." Dkt. 81 at 9. However, in IPR2022-00615 involving claim 16 of the '912 patent, Samsung claims that a POSITA would understand that a logic element that generates chip-select signals would need to be in sync with clock signals received from the PLL. Ex. 3 (Samsung IPR Pet.) at 61 ("[A] POSITA would have understood that a ***logic element*** that generates chip-select signals for the memory devices ***must be in sync with the other signals, including the clock signal, received by the memory devices from the PLL***.") (emphasis added). The original claims required a "circuit" comprising a "logic element" that receives a set of input control signals, including a "chip-select signal," and that the circuit "generat[e] a set of output control signals in response to the set of input control signals." *E.g.*, Ex. 1 ('912 patent), 32:66-33:12 (claim 1); *see also* 34:33-45 (claim 15); 35:45-57 (claim 28); 36:49-53, 36:62-66 (claim 39: "the plurality of output signals comprising . . . the first number of chip-select signals"). As indicated throughout the specification, the logic element generates chip-select signals for the memory devices. *See, e.g.*, *id.*, 7:35-8:64; Fig. 1A-1B (depicting logic element 40 as receiving and transmitting chip-select (CS) signals to SDRAMs). Thus, under Samsung's view in IPR, a POSITA would have understood that the logic element as originally claimed received a clock signal from the PLL.

2. **The "register" Amendment**

Netlist also amended the claims to add the "register" limitation below:

> wherein the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element.

Dkt. 81-01 at 48.

Samsung first argues that the requirement that the register receive, buffer, and transmit specific signals affected a substantive change. Dkt. 81 at 9. However, prior to reexamination, Netlist and Google had agreed that the term "register" means "a circuit component or components that ***receive, buffer, and transmit signals***." Dkt. 81-09 at 8 (emphasis added). The original claims recited a "circuit," comprising a "logic element" and a "register," which responds to a "command signal" and "input control signals." *E.g.*, Ex. 1 ('912 patent), 32:66-33:15 ("the circuit comprising a logic element and a register . . . wherein the circuit further responds to a first command signal and the set of input control signals from the computer system"); *see also* 34:33-48 (claim 15), 35:45-63 (claim 28), 36:48-59 (claim 39). As Samsung's IPR expert concedes, a POSITA would understand that the function of a "register" is to register the received control and address signals. Ex. 4 (Wolfe Decl. in IPR2022-00615) at p. 74 (pointing to contemporaneous JEDEC standards "showing memory modules with ***registers for registering the received control and address signals***") (emphasis added). The specification is in accord. Ex. 1 ('912 patent), 5:31-36 ("The register 60 receives and buffers a plurality of control signals, including address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices 30."), 7:43-53, Fig. 1A (register 60 depicted as receiving signals

including bank address signals BA_0-BA_m and address signals A_0-A_n).

Samsung also argues that the requirement that the "plurality of row/column address signals received by the register are separate from a row address signal received by the logic element" affected a substantive change. Dkt. 81 at 9. However, the original claims required the memory module to receive a "command signal," which Netlist and Google previously agreed means "a signal that initiates a predetermined type of computer operation, such as read, write, refresh or precharge." Dkt. 81-09 at 8. According to Samsung's IPR petition, these commands would necessarily require a row address signal as part of the command code. Ex. 3 (Samsung IPR Pet.) at 45-46 (arguing that per JEDEC standard, "to perform a read or write operation, the JEDEC standard . . . first requires a Bank Activate command ***with the row and bank address signals***") (emphasis added). It would also be understood that the address signals received by the "register" and "logic element" are separate. *See* Figs 1A-1B (depicting register as receiving A_0-A_n, and logic element as receiving A_{n+1}).

3. **The "logic element" Amendment**

Netlist also added language regarding the logic element's operation to the claims, for example:

> wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal.

Dkt. 81-01 at 49 (claim 1). Near identical additions were made to claims 15, 28, and 39. *Id.* The original claims required a logic element that receives a "set of input control signals" and that the claimed circuit comprising the logic element "generat[es] a set of output control signals in response to the set of input control signals." Ex. 1 ('912 patent), 32:66-33:12 (claim 1); *see also id.*, 34:34-45 (claim 15), 35:45-58 (claim 28), 36:49-63 (claim 39). The original claims also required that the output control signals "correspond[] to" or are "configured to control" the DDR memory devices. *See, e.g.*, *id.*, 33:12-14; 34:45-47; 35:59-62. In the context of DDR memory devices, such output control signals include chip-

select signals to select the ranks of DDR memory devices for operation. *See* Ex. 3 (Samsung IPR Pet.) at 29 ("A POSITA would have understood . . . that the chip-select signal was designed to select ranks" of DDR memory devices); *see also* Ex. 1 ('912 patent), 36:66-37:4.

Samsung argues that the amended claims now require the control signals be generated in response to signals (i)-(iv). Dkt. 81 at 9-10. However, the original claims recited signals including (i)-(iii) as part of the "input control signals." *See* Ex. 1 ('912 patent), 33:1-33:16 (claim 1); 34:36-48 (claim 15); 35:48-50 (claim 28); 36:55-59 (claim 39). And as discussed above, according to Samsung, a POSITA would understand that to generate chip-select signals, the logic element required a clock signal from a PLL, *i.e.*, signal (iv). Ex. 3 (Samsung IPR Pet) at 61; *supra* 6-7. The specification likewise makes clear that the logic element receives signals (i)-(iv) and generates chip-select signals in response. Ex. 1 ('912 patent), 6:55-63 (logic element of Figs. 1A and 1B "receives a set of input control signals, which includes address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) . . . . In response to the set of input control signals, the logic element 40 generates a set of output control signals which includes address signals and command signals"), 7:36-53; Figs. 1A-1B.

Samsung also suggests that the logic element amendment was substantive because "Netlist and the PTAB relied on this added functionality to distinguish the prior art during reexamination." Dkt. 81 at 10. The N.D. Cal. Court similarly placed emphasis on this fact. Dkt. 81-08 at 23-25 (emphasizing that the "added limitations were crucial to the allowance of the claim because they overcome rejections based on Amidi and Dell-2"). But "[w]hen claims are amended during reexamination following a rejection based on prior art, the claims are not deemed substantively changed as a matter of law. There is no per se rule." *Laitram Corp. v. NEC Corp.*, 952 F.2d 1357, 1362-63 (Fed. Cir. 1991). While relevant, the fact that this limitation was argued to overcome the prior art is not dispositive, because if it were, virtually all amendments would trigger intervening rights. *Kaufman*

Co., Inc. v. Lantech, Inc., 807 F.2d 970, 978 (Fed. Cir. 1986) (rejecting accused infringer's argument that "any amendment made during the reexamination proceeding is substantive and therefore automatically entitles the infringer to an intervening right").

C. Samsung's Identification of Accused Products is Deficient

Samsung's proposed date of February 8, 2021 as the date on which absolute intervening rights accrue is inconsistent with the language of pre-AIA § 316(a): "In *inter partes* reexamination proceeding under this chapter, when the time for appeal has expired ***or any appeal proceeding has terminated***, the Director shall issue and publish a certificate [of reexamination]." Pre-AIA § 316(a) (emphasis added). The Federal Circuit affirmance occurred on June 15, 2020. 810 F. App'x at 902. Only products used or purchased prior to June 15, 2020 could be subject to intervening rights.

Samsung has also not properly disclosed all the Accused Products. [redacted] *MOSAID Techs. Inc. v. Micron Tech., Inc.*, 2008 WL 11344767, at *6 (E.D. Tex. Jan. 29, 2008) (defendants could "easily determine the extent of the accused devices" based on identification of products by names that "the industry uses for the devices, e.g. SDRAM, DDR, DDR2, DDR3…."). [redacted] Dkt. 81-07, ¶ 12.

VI. CONCLUSION

For the foregoing reasons, Samsung's motion for partial summary judgment should be denied.

Dated: July 6, 2023

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that a copy of the foregoing document was served on all counsel of record for Samsung through the Court's CM/ECF system on July 6, 2023.

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